CSE140 Discussion

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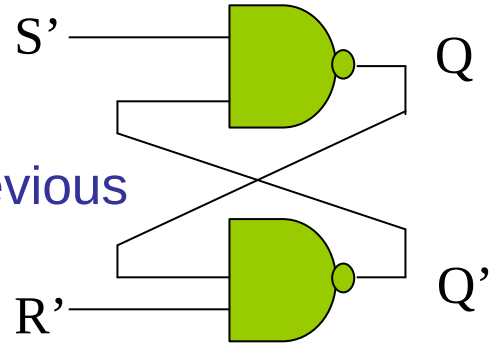
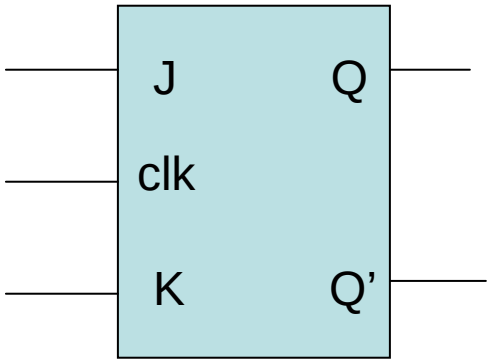
3.4 Sequential circuit check

S	R	Q	Q’	
0	0	Q_{prev}	Q'_{prev}	Retain previous state
0	1	0	1	reset
1	0	1	0	set
1	1	1	1	invalid

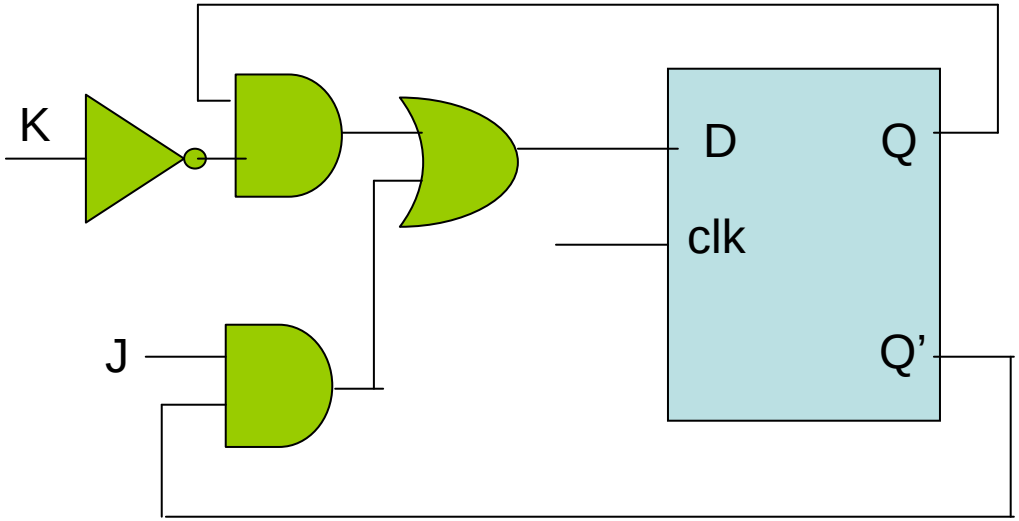


Still an SR latch

3.7 Flip-flop conversion: D➔JK

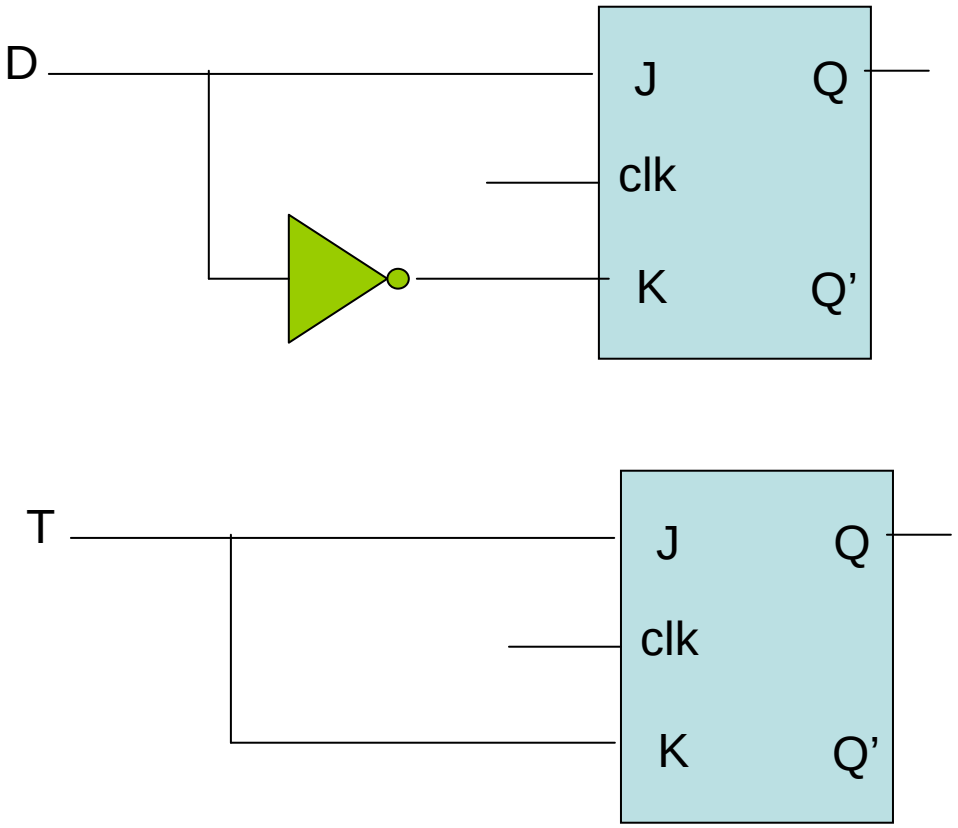


J	K	Q	Q'
0	0	Q_{prev}	Q'_{prev}
0	1	0	1
1	0	1	0
1	1	Q'_{prev}	Q_{prev}



D	Q	Q'
0	0	1
1	1	0

3.7 Flip-flop conversion: JK➔D&T



Question:
D ➔ T
T ➔ D

Sequential circuit design flow

Step 1:

Circuit specification ➔ FSM

Step 1:

FSM ➔ Next state table. The table should show the present states, inputs, next states and outputs.

Step 2:

State encoding. If you have n states, your binary codes will have at least $\lceil \log_2 n \rceil$ digits, and your circuit will have at least $\lceil \log_2 n \rceil$ flip-flops.

Step 3:

Select flip-flop and create flip-flop excitation table. For each flip-flop and each row of your state table, find the flip-flop input values that generate the correct next state.

Step 4:

Find simplified equations for the flip-flop inputs and the outputs. You can use Kmap to derive each equation

Step 5:

Build the circuit!

3.26 FSM design

Specification:

Input: A, B

Outputs: Z

$Z_n = A_n\ A_{n-1}$, if $B_n = 0$

$Z_n = A_n + A_{n-1}$, if $B_n = 1$

Is this FSM a Moore machine or Mealy machine?

Mealy machine, as the output depends on the input value

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$Z_n = A_n A_{n-1}$, if $B_n = 0$

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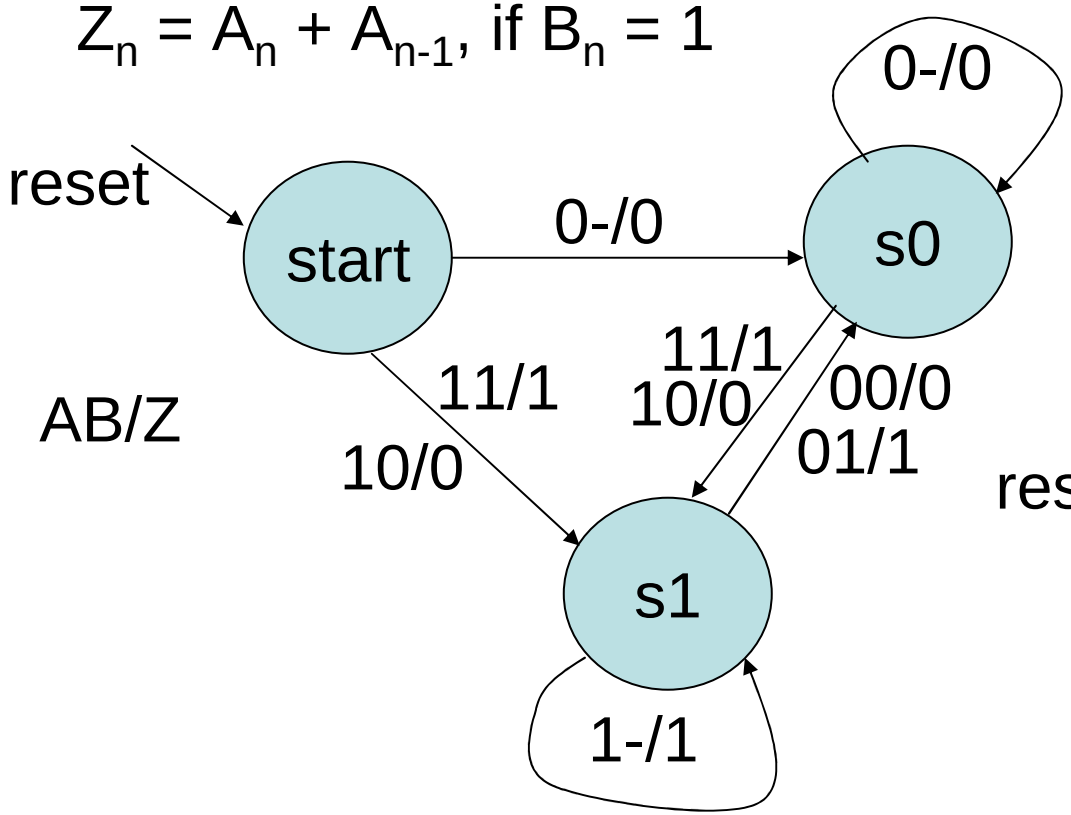
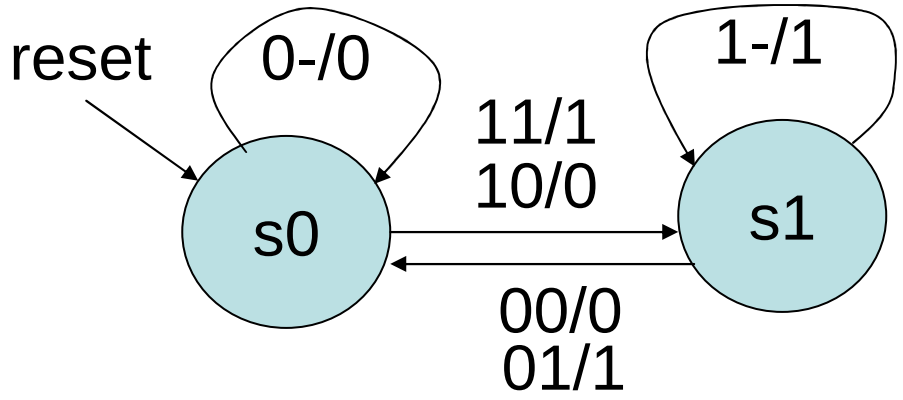
Draw the FSM diagram

Idea: need two states for memorizing A_{n-1}



Can it be optimized?

No difference between Start & S0. They can be merged!



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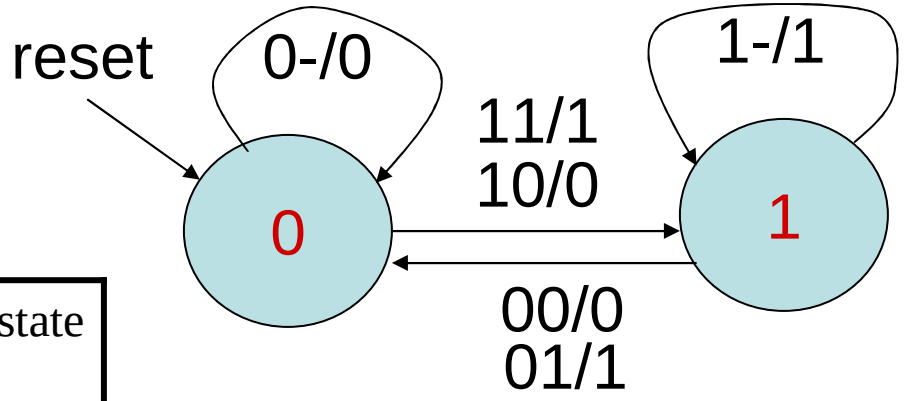
State encoding



A	B	Current state	Next state
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Next state equation:

$Q_{next} = A$

3.26 FSM design

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Outputs: Z

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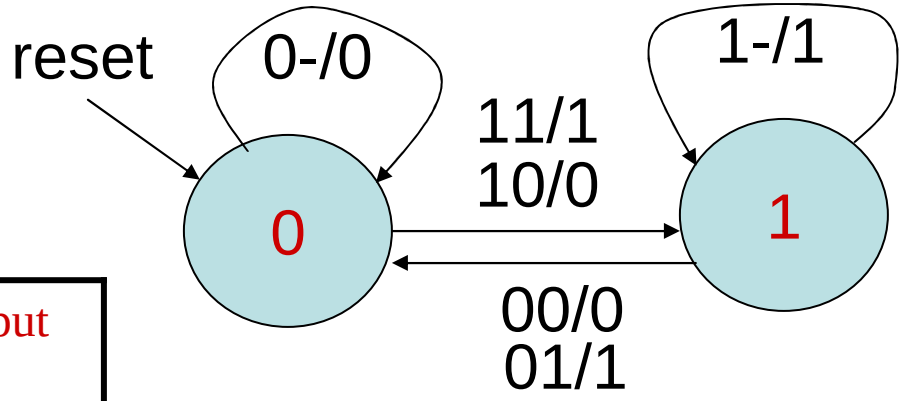
$Z_n = A_n + A_{n-1}$, if $B_n = 1$

A	B	Current state	output
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

State encoding



AB

$Q_{current}$	00	01	11	10
0	0	0	1	0
1	0	1	1	1

Output equation:

Z = AB+BQ+AQ

3.26 FSM design

Specification:

Input: A, B

Outputs: Z

$Z_n = A_n A_{n-1}$, if $B_n = 0$

$Z_n = A_n + A_{n-1}$, if $B_n = 1$

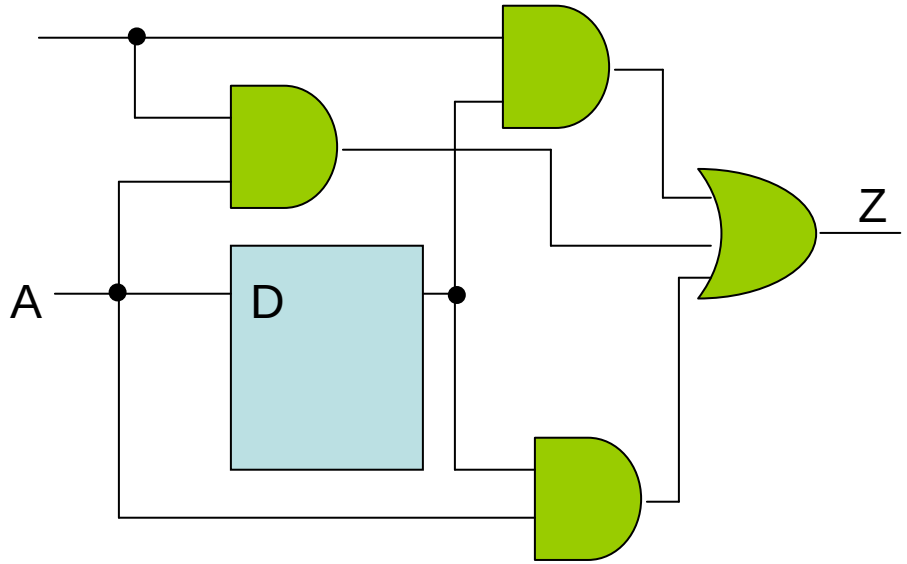
Next state equation:

$Q_{next} = A$

Output equation:

$Z = AB+BQ+AQ$

Use D flip-flop



Question:
How to design the circuit using JK flip-flop?