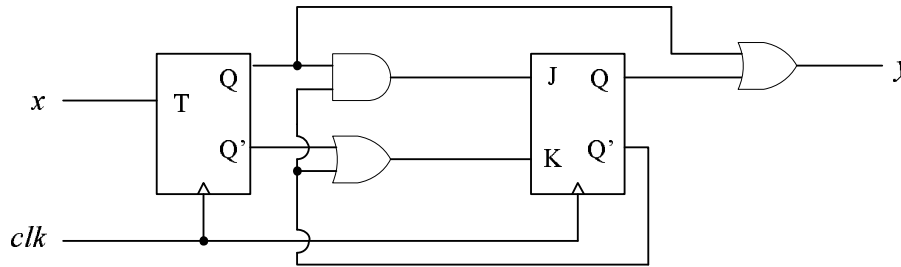# CSE140 Exercise 4

(I) (Flip-Flops) Implement a JK flip-flop with a T flip-flop and a minimal AND-OR-NOT network. Let us assume that the complements of J, K and Q signals are available. Draw the logic diagram to show your design.

(II) (Design Specification) Write the state table of the sequential circuit as the following figure.


(III) A state machine is described by the following state equations.

$$Q_1(t+1) = Q_0'(t)x(t),$$
$$Q_0(t+1) = Q_1(t) + x'(t),$$
$$y(t) = Q_1(t)Q_0(t).$$

(1). Write the state table.

(2). Design the system with two JK flip-flops and a minimal AND-OR-NOT network.

IV. In the following circuit, each flip flop has a setup time of 75ps, a hold time of 30ps, a clock-to-Q maximum delay of 80ps, and a clock-to-Q minimum delay of 55ps. Each AND gate has a propagation delay of 70ps and a contamination delay of 55ps, while the NOR gate has a propagation delay of 85ps and a contamination delay of 65ps.
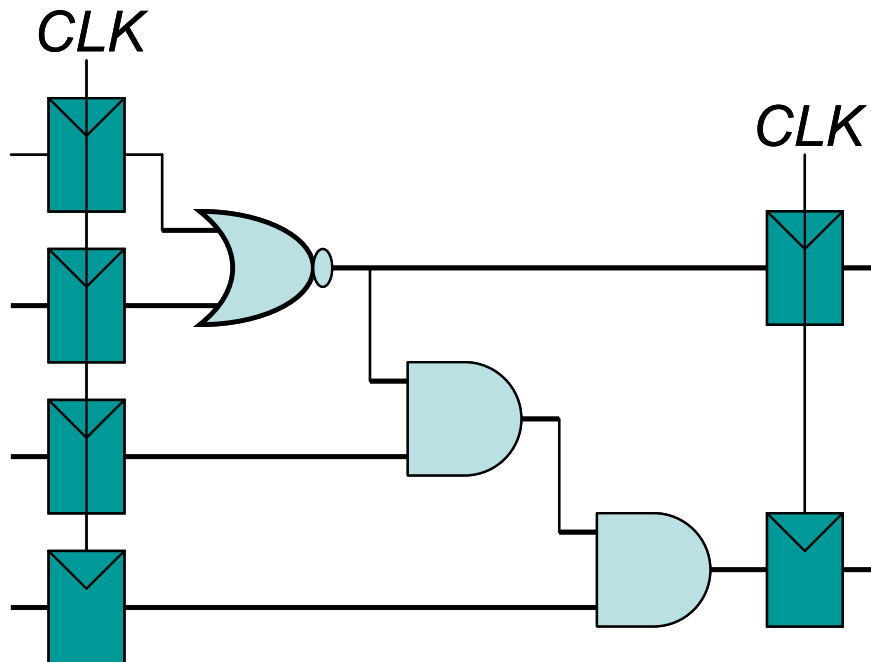
a) If there is no clock skew, what is the maximum operating frequency of this circuit?

b) How much clock skew can the circuit tolerate before it might experience a hold time violation?

c) Redesign the circuit so that it can be operated at 3GHz frequency. How much clock skew can your circuit tolerate before it might experience a hold time violation?

V. Given a three-input Boolean function $f(a, b, c) = \sum m(0, 2, 4, 6, 7) + \sum d(1)$.

a. Implement the function using a minimal network of 2:4 decoders and OR gates.

b. Implement the function using a minimal network of 4:1 multiplexers.

c. Implement the function using a minimal network of 2:1 multiplexers.