CSE140 Exercies 4

(I) (Flip-Flops) Implement a JK flip-flop with a T flip-flop and a minimal AND-OR-NOT network. Let us assume that the complements of J, K and Q signals are available. Draw the logic diagram to show your design.

Step 1: write the next state table

JK flip-flop next state table

J	K	$Q_{current}$	Q_{next}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

T flip-flop excitation table

T	$Q_{current}$	Q_{next}
0	0	0
0	1	1
1	0	1
1	1	0

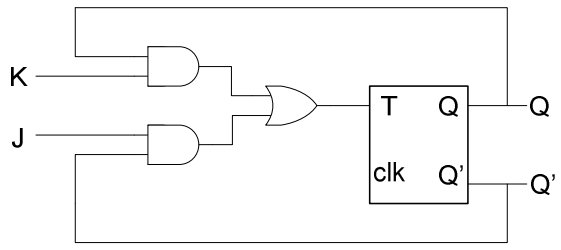
Step 2: derive the excitation table from the next state tables

Excitation table

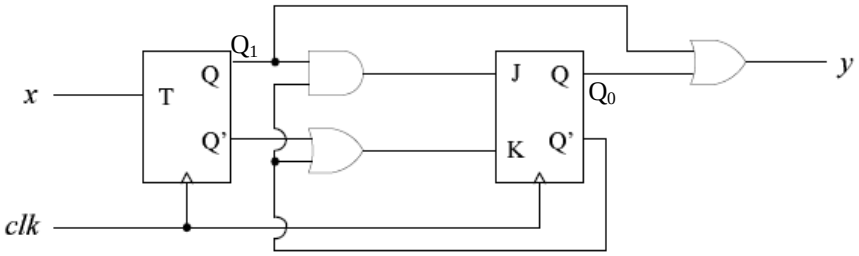
J	K	$Q_{current}$	T
0	0	0	**0**
0	0	1	**0**
0	1	0	**0**
0	1	1	**1**
1	0	0	**1**
1	0	1	**0**
1	1	0	**1**
1	1	1	**1**

Step 3: derive next state logic

T = JQ’ + KQ



(II) (Design Specification) Write the state table of the sequential circuit as the following figure.



From the circuit we directly get

T = x

J = Q_1Q_0'

K = Q_1'+Q_0'

y = Q_1+Q_0

We use these equations to get $Q_1(t+1)$ and $Q_0(t+1)$:

Q_1 Q_0	T	$Q_1(t+1)$	J	K	$Q_0(t+1)$
00	0	0	**0**	**1**	0
00	1	1	**0**	**1**	0
01	0	0	**0**	**1**	0
01	1	1	**0**	**1**	0
10	0	1	**1**	**1**	1
10	1	0	**1**	**1**	1
11	0	1	**0**	**0**	1
11	1	0	**0**	**0**	1

Finally, we get the state table:

Q_1 Q_0	Next sate		Output (y)	
	X=0	X=1	X=0	X=1
00	00	10	0	0
01	00	10	1	1
10	11	01	1	1
11	11	01	1	1

(III) A state machine is described by the following state equations.

$$Q_1(t+1) = Q_0'(t)x(t),$$
$$Q_0(t+1) = Q_1(t) + x'(t),$$
$$y(t) = Q_1(t)Q_0(t).$$

(1). Write the state table.

$Q_1\ Q_0$	Next sate		Output (y)	
	X=0	X=1	X=0	X=1
00	01	10	0	0
01	01	00	0	0
10	01	11	0	0
11	01	01	1	1

(2). Design the system with two JK flip-flops and a minimal AND-OR-NOT network.

Derive the excitation table:

X	Current state ($Q_1\ Q_0$)	Next state ($Q_1\ Q_0$)	J_1	K_1	J_0	K_0
0	00	01	0	-	1	-
0	01	01	0	-	-	0
0	10	01	-	1	1	-
0	11	01	-	1	-	0
1	00	10	1	-	0	-
1	01	00	0	-	-	1
1	10	11	-	0	1	-
1	11	01	-	1	-	0

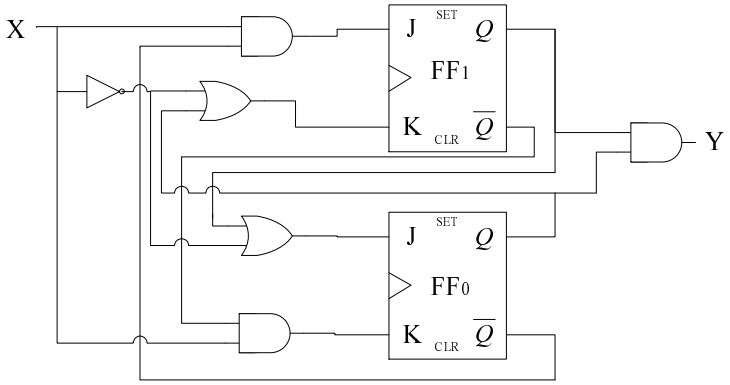
Derive the next state logic:

$J_1 = Q_0'\ X$

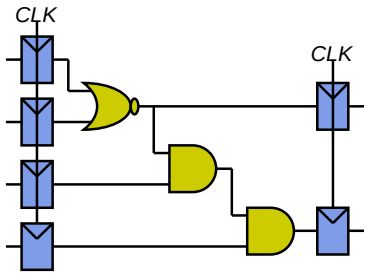
$K_1 = X' + Q_0$

$J_0 = Q_1 + X'$

$K_0 = Q_1'\ X$



(IV) In the following circuit, each flip flop has a setup time of 75ps, a hold time of 30ps, a clock-to-Q maximum delay of 80ps, and a clock-to-Q minimum delay of 55ps. Each AND gate has a propagation delay of 70ps and a contamination delay of 55ps, while the NOR gate has a propagation delay of 85ps and a contamination delay of 65ps.



a) If there is no clock skew, what is the maximum operating frequency of this circuit?

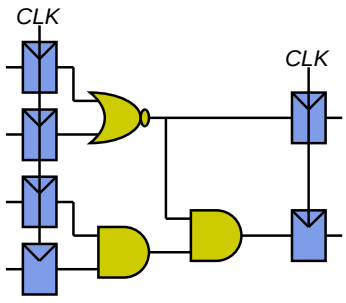
The constraint is: $T_c \geqslant T_{pcq} + T_{pd} + T_{setup}$
In this circuit, the longest path contains the NOR and two AND gates. Therefore, we have:
$T_c \geqslant 80+ 85 + 2*70 + 75 = 380$ ps → Max Frequency = 1/380ps = 2.63 GHz.

b) How much clock skew can the circuit tolerate before it might experience a hold time violation?

The constraint is: $T_{ccq} + T_{cd} \geqslant T_{hold} + T_{skew}$
In this circuit, the shortest path contains only the AND gate at the bottom. Therefore we have:
$55 + 55 \geqslant 30 + T_{skew}$ → $T_{skew} \leqslant 80$ ps

c) Redesign the circuit so that it can be operated at 3GHz frequency. How much clock skew can your circuit tolerate before it might experience a hold time violation?

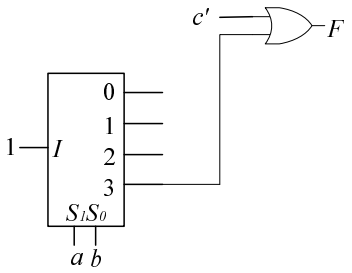
We can put the second and before the first end since ((a+b)'c)d = (a+b)'(cd)



Now the longest path contains one NOR and one AND gate.
$T_c \geqslant 80+ 85 + 70 + 75 = 310$ ps → Max Frequency = 1/310ps = 3.22 GHz.
The shortest paths contains only the NOR gate.
$55 + 65 \geqslant 30 + T_{skew}$ → $T_{skew} \leqslant 0$ ps

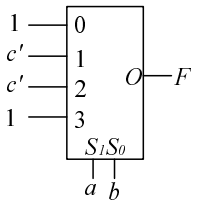
(V) Given a three-input Boolean function f(a; b; c) = Pm(0; 2; 4; 6; 7) + Pd(1).
a. Implement the function using a minimal network of 2:4 decoders and OR gates.

F = c'+ab



b. Implement the function using a minimal network of 4:1 multiplexers.

F = c'(a'b'+a'b+ab')+ab = c'(a'b+ab')+ab // utilize the don't care a'b'c



c. Implement the function using a minimal network of 2:1 multiplexers.