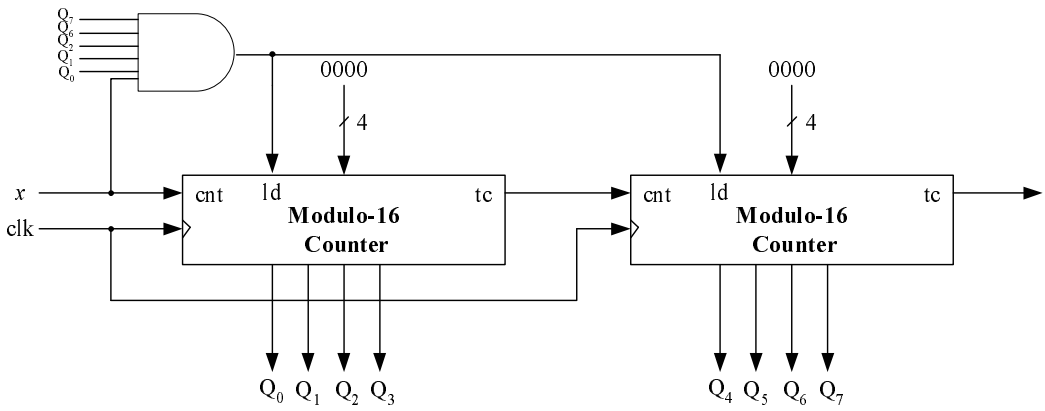
IV(1). Design a modulo–200 counter with a repeated output.

We know that $2^7 < 200 < 2^8$, so we need 8 bits to represent 0 – 199. A modulo–16 counter have 4 bits output, so two such counters are enough, with one representing the least significant 4 bits, and the other representing the most significant 4 bits.

The terminal count (tc) signal of the first counter will be sent to the enable port (cnt) of the second counter; consequently, the second counter will count once when the first counter reaches 1111. Thus the carry could be perform correctly in this way.

Since we want to count the numbers from 0 – 199, the load (ld) signal should be sent to both counters to load 0000 when the number counts to 199, which is 1100 0111. So we should use an AND gate which takes the signal of Q_7, Q_6, Q_2, Q_1, Q_0 together with the input signal x to generate the load signal for both counters.

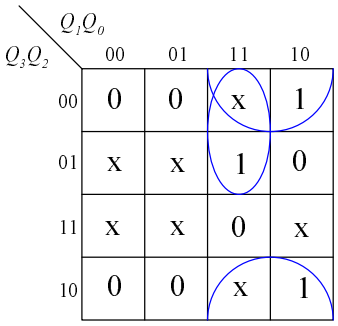


IV(2). Design a counter with a repeated output sequence 15, 0, 1, 2, 8, 9, 10, 6, 7, with a modulo–16 counter and a minimal combinational network. Write the Boolean expression and draw the schematic diagram.

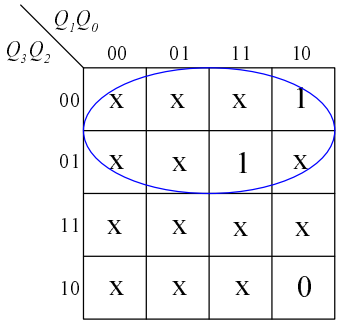
From the given the sequence, we can determine the load bit L and the values I_3, I_2, I_1, I_0 that will be loaded to the counter, according to the current output Q_3, Q_2, Q_1, Q_0. The truth table is as follows:

ID	Q_3	Q_2	Q_1	Q_0	L	I_3	I_2	I_1	I_0
0	0	0	0	0	0	x	x	x	x
1	0	0	0	1	0	x	x	x	x
2	0	0	1	0	1	1	0	0	0
3	0	0	1	1	x	x	x	x	x
4	0	1	0	0	x	x	x	x	x
5	0	1	0	1	x	x	x	x	x
6	0	1	1	0	0	x	x	x	x
7	0	1	1	1	1	1	1	1	1
8	1	0	0	0	0	x	x	x	x
9	1	0	0	1	0	x	x	x	x
10	1	0	1	0	1	0	1	1	0
11	1	0	1	1	x	x	x	x	x
12	1	1	0	0	x	x	x	x	x
13	1	1	0	1	x	x	x	x	x
14	1	1	1	0	x	x	x	x	x
15	1	1	1	1	0	x	x	x	x

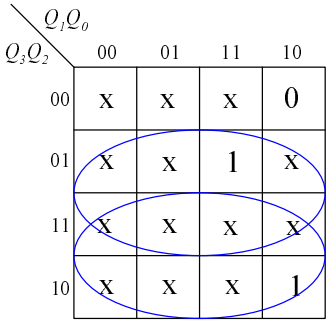
Hence, $L = Q_2'Q_1 + Q_3'Q_1Q_0$, $I_3 = Q_3'$, $I_2 = I_1 = Q_3 + Q_2$, $I_0 = Q_2$. The K-maps are shown as follows.



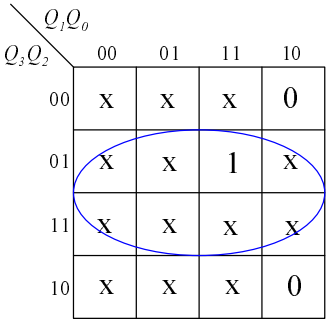
L



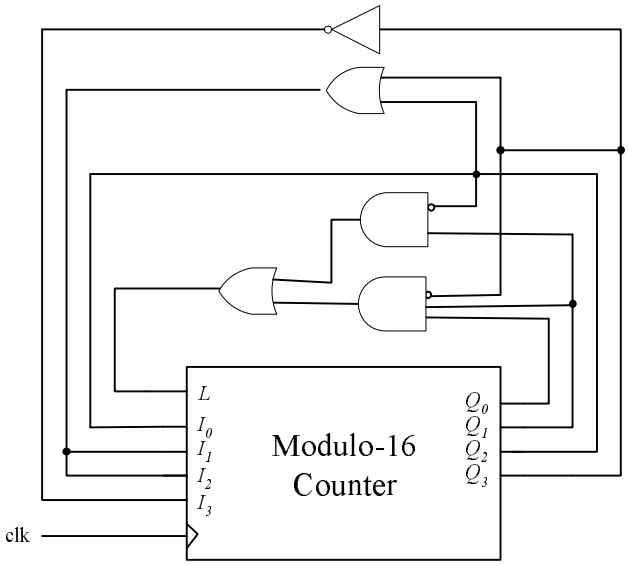
I_3



I_2, I_1



I_0



V. Design a counter with a repeated output sequence 0, 1, 2, 4, 5, 6, 3, with a modulo–8 counter and a minimal AND-OR-NOT network. Write the Boolean expression and draw the schematic diagram.

From the given the sequence, we can determine the load bit L and the values I_2, I_1, I_0 that will be loaded to the counter, according to the current output Q_2, Q_1, Q_0. The truth table is as follows:

ID	Q_2	Q_1	Q_0	L	I_2	I_1	I_0
0	0	0	0	0	x	x	x
1	0	0	1	0	x	x	x
2	0	1	0	1	1	0	0
3	0	1	1	1	0	0	0
4	1	0	0	0	x	x	x
5	1	0	1	0	x	x	x
6	1	1	0	1	0	1	1
7	1	1	1	x	x	x	x

Hence $L = Q_1$, $I_2 = Q_2'Q_0'$, $I_1 = Q_2$, $I_0 = Q_2$ (from K-Maps).