CSE140L Exercise

1. Use CMOS complementary logic to implement the following functions. Draw the circuit to show your design.

a) f(a) = a’.

b) f(a,b) = (ab)’.

c) f(a,b,c) = (ab+c)’.

2. Design a 3-bit asynchronous counter with D flip-flops.
   a) Show the logic diagram.
   b) Suppose we want to increase the bit width, what is the limiting factor of the counter size? Explain your solution.

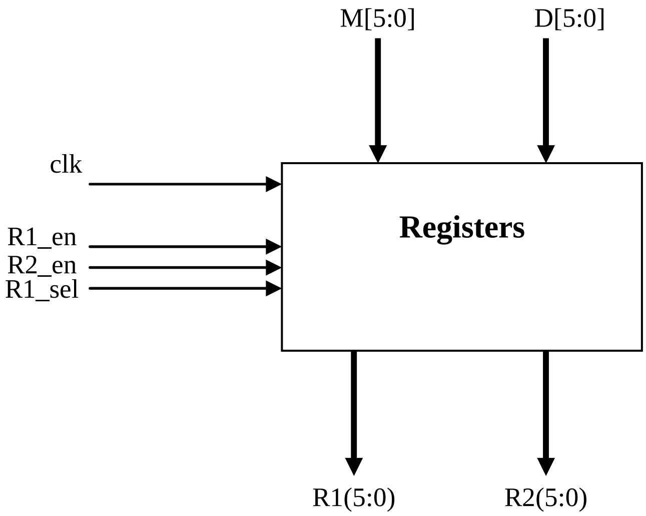
3. Given a Mealy machine as described by the following state table. Transform the Mealy machine to a Moore machine. Write the state table.

PS	x=0	x=1
A	A, 1	B, 0
B	C, 1	F, 1
C	A, 1	E, 0
D	B, 0	E, 0
E	E, 1	D, 1
F	E, 0	F, 0
	NS, z	

4. Assume a computer system has a simple instruction set described as follows:

Command	**2-bit Instruction**	**6-bit Data**	**Description**
Move1	00	$m_5m_4m_3m_2m_1m_0$	Move data $m_5m_4m_3m_2m_1m_0$ to register R1.
Move2	01	XXXXXX	Move data in register R1 to register R2.
Add	10	XXXXXX	Add the content of R1 and R2 and store the result back to R1.
Shift	11	XXX$m_2m_1m_0$	Left shift (NOT rotate) the content of R1 by $m_2m_1m_0$ bits and store the result back to R1.

The registers block has two 6-bit input data ports: M[5:0] and D[5:0]; the former is from the memory source and the latter is from the datapath. The outputs of R1 and R2 are connected to datapath as well as data port D[5:0]. However, the communication between R1 and R2 can be performed inside the registers block. The Control signals R1_en and R2_en are the enable signals for R1 and R2 respectively. Control signal R1_sel is used to select the sources of R1.



a) Complete the following table which describes the function of the registers block:

R1_en	R2_en	R1_sel	clk	R1[5:0]	R2[5:0]
1	0	0	↑	M[5:0]	No Change
1	0	1	↑		
0	1	X	↑		

b) Write the truth table of the instruction decoder (control subsystem). Use the 2-bit instruction as inputs and R1_en, R2_en, R1_sel as outputs.

c) Complete the following program that performs the multiply-by-33 function. By the end of the program you should have data 33* $a_5a_4a_3a_2a_1a_0$ stored in R1 (assume no overflow; you must write out ALL the instructions)..

move1 $\mathbf{a_5a_4a_3a_2a_1a_0}$ -- move data $a_5a_4a_3a_2a_1a_0$ into R1